Guy Regev

An expert engineer and a leader who loves intractable problems.

I am a self-driven veteran of the ASIC/FPGA AND IC design in the tech industry, with over 20 years of experience across all technical disciplines of chip/ASIC or IC design as well as FPGA design, extensive hands-on experience as well as managing cross-functional international teams through all aspects of the chip design through production. I have a proven track record of successful, time-crunched seemingly "impossible" tape-outs of flagship products. When I'm not doing chips, I hack computer vision and deep learning to fit on platforms such as RasPi. Expert Witness for cases that involve mobile devices, GPS, semiconductor devices, electronic design automation (EDA), hardware, chips, IC Design, SoC Design or FPGA design, as well as software, and embedded firmware.

Address:
Los Angeles, CA

Contact information:
guy.regev@ieee.org
(209) 222-8685

Summary of qualifications:

Architecture and RTL Design and verification: Extensive hands-on experience with *architecture* of many SoCs and complex blocks as well as *RTL* writing and *functional verification* for both ASIC and FPGA. Extreme knowledge in design for PPA, i.e. *architecting an SoC to meet timing, power and area budgets* from the get-go, making the rest of the flow almost a push button.

Physical Synthesis: Extensive hands-on experience with ramping up comprehensive *physical synthesis* flows from scratch

Timing Closure and PPA: Extensive hands-on experience with *physical design, timing closure, and tape-out sign-off.*

Methodology: Extensive experience with the entire ASIC design methodology (as well as FW design). Led and did significant hands-on work with developing many methodologies and flows from scratch from front-end to back-end, with emphasis on flows and methodologies that will most likely yield a *bug-free device that is right the first time.*

Over 20 years of experience in developing a range of product areas: networking, wireless/cellular communications, Switch ASICs CPUs, DSPs, FPGAs, software, firmware, system, IPs, CAD/SW tools.

Over 12 years of experience in senior management of design and production of integrated circuits, FPGAs, SW, and CAD tools, from conception to mass-production

Built multiple international development teams, some from scratch, and was able to quickly form cohesive functional teams, while building best in class design flows.

Direct management of all parts of the Silicon/HW development and indirect management (as head of program management) of HW, SW, FW, CAD, QA: Including: architecture, design, functional verification, DFT, physical design, CAD, post-si ATE and bench testing, characterization, package/board development, test development and bring-up, operations (PT/PE)

Extensive hands-on experience with the following tools:

- Verilog and RTL design
- Functional Verification
- Perl scripting
- Python
- Git/CVS/Mercurial
- Tcl
- Timing constraints design
- Running computer vision in real time on platforms like Raspberry Pi

Proficient hands-on experience with: lint, CDC, formal, power estimation tools, DFT tools, ATPG tools

Extensive **Intellectual Property** experience including patent development, analysis, licensing, and strategic positioning. Holds 6 patents.

Many successful unique complex, SoCs brought from concept to volume production in multiple companies. Many more tape-outs, shrinks, and product derivatives were brought to production. Covering 65nm down to 10nm processes

Negotiated agreements for the purchase of EDA/CAD tools silicon, IP, other vendors, and known foundries for over $20M.

Expert Witness in patent and liability cases that involve IC Design, Chip design, FPGA Design, hardware, software, embedded firmware, EDA/CAD tools.

Consulting and advising companies on patent strategy, product positioning and development in the areas of IC Design, FPGA Design and software/embedded firmware design, as well as leadership coaching (how to hire and build cohesive development teams that follow a strict methodology that enable on-time deliveries with high quality (minimal bugs).

Experience

Apr 2019 – Now: Owner and Expert Witness at GR Technologies, LLC.

- My firm employs several expert witnesses in various areas such as networking, wireless/wired communications, cellular communications, software, firmware, hardware, ASIC, FPGA, semiconductors, radar signal processing, computer vision and image processing, signal processing, algorithms, optics and optical systems, lidars, cameras, sonar, ultra-sound, optical communications and devices, display technologies inc. touch screens, OLED, LCD, EPD, LCD, TFT backplanes and more, Fluid and thermal flow and analysis, RF and antenna design and remote and wearable sensors.
- Personally, helping my clients with patent and liability cases that involve Semiconductors, FPGAs, Hardware, Software, Embedded Firmware and EDA/CAD tools.
- Pre-litigation: Patent infringement and validity analysis. Hardware and software code reverse engineering and reviews – hardware soft (x-ray/CT imaging) and hard teardowns, software extraction out of processors and micro-controllers, software/firmware reverse engineering.
- Doing hardware and software reverse engineering on cases for Latham & Watkins. Produced many patent analysis reports, hardware and software reverse engineering reports.
- Product Liability Cases: Point of failure analysis - did a failure happen due to hardware, software. Analyze and identify the point of failure.
- Participated in 28 hours of SEAK various Expert Witness training courses.

Dec 2017 - Now: Chief Engineer & Managing Partner at AlephZero Consulting, LLC.

- AlephZero Consulting, LLC is a unique consultancy with extreme experience in designing complex algorithm design, chip/FPGA design as well as embedded (real-time) software/firmware design. Our customers range from chip design companies, automotive companies, automotive radar and lidar makers, retail automation companies, financial institutions and more.
- Leading the hardware and embedded software/firmware design of our consultancy.
- Hands-on chip design work for fabless semiconductor companies in the areas of Architecture, SoC Architecture, RTL Design, Verification, early power/area estimation, early floor planning and PPA calculations, flow optimizations, physical synthesis, P&R and timing closure.
- Developed real-time image object detector using neural networks on a Raspberry Pi as an initial prototype and proof of concept for a customer
- Perl and Python scripting for several customers as part of the overall help with prototyping and chip design

2015 - Nov 2017: Director of VLSI, Rockley Photonics Inc.

- Director of VLSI at Rockley Photonics, a well-funded start-up company that designs and manufactures opto-electrical switch ASICs for data centers. Responsible for the entire VLSI development in the company (digital and analog).
- Managed the design of the company's flagship large and complex switch ASIC (~200mm sq), Topanga-1 - a 1.2TB throughput switch ASIC with in-house analog mixed-signal periphery to enable on-package optical/electrical integration
- Built a fully functional digital and analog team from scratch.
- Established a complete design flow (based on Cadence, Synopsys' and Mentor tools) from scratch.
- Managed both internal teams as well as all the external teams and partners involved in the design of this device (>40 engineers)
- Responsible for company-wide program management – Program Management reports to me.
- Chip was done in the 28nm HPC+ process at TSMC – the device was successfully taped-out and came back from fab fully functional on the first tape-out.
- Hands-on participation in architecture, design for PPA, flow development (Perl Python, Tcl), physical design and timing closure.
- Negotiated and put together many partner relationships that included direct access to TSMC (rare for a start-up) as well as design EDA tools, IP and services agreements with companies like Synopsys, Cadence, Mentor Graphics and other partners

2011-2015: Senior Director of VLSI Engineering, Mindspeed Technologies (acquired by Intel in 2014)

- Managed all the projects/products of Intel's wireless cellular base-station products – overall 2 existing chip families and one next-generation family that's currently being

designed.

- Managed and hands-on participation in the development from the concept of T2200/T3300 devices, the company's wireless small-base-station baseband processor flagship products.
    - Managed a big team >50 engineers
    - The design was done in 32nm low-power process at Samsung.
    - The device supports dual-mode LTE and 3G (UMTS/HSPA+), 4x4 MIMO, 64 users
    - The device included several cutting-edge processors and DSPs which were timing-closed to aggressive frequencies
    - Devices are now in full production and being shipped to many customers by Intel
- Managed and participated in hands-on the development of next-generation product development, T3400
    - Design is being done in Intel's 14nm low-power process
- Managed and participated hands-on the aggressive P&R and timing closure of the Intel UK (used to be Picochip) recent devices, last of which was implemented at 40nm at TSMC after they missed their tape-out date. Helped to get the design closed and ready for tape-out quickly
- Put in many new cutting-edge design-flows in place and completely transformed Mindspeed's design flows to enable schedule consistency and predictability, high quality, right-the-first-time, big free chips.

2008-2011: Manager IC-Design, Broadcom
ASIC Group Manager, Percello **(was acquired by Broadcom)**

- Managed the VLSI department of Broadcom Israel (Percello – a fabless semiconductor company which was acquired by Broadcom during 2010) and reported directly to the Sr. Director of Engineering in Percello.
- Greatly contributed to Percello's success and acquisition process – both through on-time technical deliveries, as well as with thorough documentation and presentations and participated in the acquisition due-diligence process.
- Managed the development of the next generation project in Broadcom – LTE baseband processor for small cells. This is a cross-site project which involves many of Broadcom's teams.
- Provided direct technical counsel to the company's executive leadership on business development issues and product roadmap.
- Managed and hands-on participation in the silicon development of Percello's PRC6000 SoC IC, the company's flagship product. Managed a large cross-site team in the process. Led it from conception to a successful tape-out and mass-production.
- PRC6000 was a 3G (UMTS/HSPA+) femtocell baseband (small cellular base station) processor in the 65nm low-power process node, integrating a CPU processor at 500Mhz and DSP core at 300MHz
- Led entire project planning and execution – from concept and architecture to volume

production.

- Full design cycle in less under one year, from system definitions to tape-out.
- Successful test program ramp, including Tester selection, test program development, test vendor management, full characterization, process skewing, and yield management, full reliability testing (HTOL, HAST, temperature cycle, etc.)
- Directly managed mass-production including ordering engineering and production lots from TSMC, handling wafer shipments to packaging
- Chip was right the first time and is now in mass-production (single tape-out)
- Led and took part in the evaluation, definition, and development of all design flows from scratch
- Managed the development of the next generation small base-station baseband processor in Broadcom
- Filed several patents during the projects' development
- In charge of all partners, fabs, test vendors, and contractor relations and all related business negotiations
- Published an IEEE article regarding the innovative methodologies employed by the team and presented at Synopsys SNUG

2005 – 2008: Manager VLSI design, LSI/Agere Corporation, Israel

- Led several product developments in LSI which included a few silicon chips for cellular handsets (cell phones)
- In one project, I led a multi-disciplinary, cross-site (Israel and US) project of the company's roadmap. The projects consisted of the integration of two chips: a 3G UMTS modem for handsets (cellular phones) with a GSM modem while designing and adding brand new features as well as die shrink to 65nm process (first of its kind in the company)
- In the other product, managed and led a stand-alone 3G UMTS/HSDPA modem that went to a cellular phone that Samsung produced.
- Reported directly to the Sr. Director of 3G technologies design in LSI
- Managed and led the project through very successful tape-outs and bring-up to a fully-functional IC.
- All product devices were right the first time and went to production on the first tape-out.
- Led the production program bring-up and device characterization
- Managed a large international engineering team (about 40 engineers) from U.S., India, and Israel
- Responsible for all of the VLSI/ASIC design aspects, from Architecture/RTL to layout to GDSII and test vector bring-up for production readiness, bring up and testing.

2001 – 2005: Senior VLSI Engineer, Intel, Israel, and the USA

- Worked on the Centrino Duo mobile processor (Centrino Duo) – Intel's first 65nm tape-out, and first dual-core architecture.
- Gained very extensive knowledge in the complete design cycle of huge, ultra-speed VLSI projects
- Worked in Santa Clara, CA for a relocation period.
- Gained vast knowledge with high-speed architecture designs
- Designed and verified a very large block called Memory Ordering Buffer (MOB)
- Led the verification of a large group of logic blocks in the CPU called Memory Cluster
- Owned the full chip timing flow development and timing closure, to enable timing closure of a multi-core CPU running at a frequency of 3GHz
- Developed an innovative approach for dual-core full chip STA Flow optimization which reduced the full chip timing problem to a single core, thus saving months in the project's schedule, money, and resources. The solution was adopted in many projects across Intel.
- Gained valuable experience with Intel HDL and synthesis (Physical Compiler).
- Proposed a method of increasing the performance of the processor by several percent.

1998 – 2000: Senior VLSI/ASIC Design Engineer, Kerenix, Israel

- Kerenix was a startup that was trying to develop a huge ethernet electro-optical switch.
- I was responsible for the architecture, design, and verification of major blocks of the switch chip(s)
- Kerenix went bankrupt and closed-shop in 2001.

1998 – 2000: VLSI Design Engineer, Motorola Semiconductor, Israel

- Worked on "Star-Core" which was Motorola Semi's flagship DSP processor chip at the time.
- Gained extensive knowledge of DSP architectures, programming, and parallelism.
- Full verification of individual logic blocks, as well as full-chip level, using PERL and Verilog.
- Utilized various verification methods (Formal Verification, Equivalence Checking, etc.)
- Extensive DFT knowledge in all scan methods (Mux-D and LSSD), JTAG/MBIST

Education

Ben Gurion University, Israel

Bachelor of Science in Electrical and Computer Engineering *1995 – 1998*

(Finished full curriculum of B.Sc EE, plus a few M.Sc. courses in 3 years instead of 4)

- Focusing on communication systems and signal processing

Professional Associations

Senior Member of IEEE

- Senior IEEE member
- Senior Member, IEEE Consultants Network
- Senior Member, IEEE Circuits and Systems Society
- Senior Member, IEEE Communications Society
- Senior Member, IEEE Computational Intelligence Society
- Senior Member, IEEE Consumer Electronics Society
- Senior Member, IEEE Engineering in Medicine and Biology
- Senior Member, IEEE Signal Processing Society
- Senior Member, IEEE Systems, Man, and Cybernetics Society
- Senior Member, IEEE Technology and Engineering Management Society
- Senior Member, IEEE Systems Council
- Senior Member, IEEE Council on Electronic Design Automation
- Member, ACM

Advisory Boards

- **PXLIZE LLC. – Automating parental controls for digital video content using sophisticated deep learning**
- **CRadar.Ai – A paradigm shift that improves Radar's phase accuracy by orders of magnitude**

Publications

- ”A methodology for timely verification of a complex SoC,” IEEE 2009 International SoC Design Conference (ISOCC), Busan, 2009, pp. 137-140.
- "Reduction in ATE Test time for Core Wrapped (Border Sealed) blocks by Avoiding Q->SI at speed timing arcs & Interface X sources", Intel SoC Conference

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Patents

- “Generating a random number in an existing system on chip” - US8522065B2

- “System and method for line coding” - US20170230143A1
- “Synchronization and ranging in a switching system” - US20170279591A1
- “METHOD OF REMOTELY MONITORING RESPIRATION” - US 62/625,578

- “Hardware efficient system and method for load balancing using a random number” - US20180074861A1

- “Optoelectronic Switch” - GB2566248B

Additional Qualifications

- Fully-developed and proven managerial and leadership skills
- Very strong analytical and problem-solving skills
- A true self-driven hands-on innovator who uses out of the box thinking to flip problems on their heads and accomplish the "impossible"
- U.S Citizen
- Extreme knowledge in semiconductors design from circuit level to high level architecture as well as hardware and software design
- Extreme knowledge in an immense variety of ASIC/FPGA tools and processes
- Extreme hardware and software hacking abilities including control over several languages such as Perl, Python, Tcl, and platforms such as Raspberry Pi and Arduino.
- Proven ability to manage and lead large-scale multi-disciplinary and multi-site projects to aggressive and on-time and high-quality deliveries (Single tape-out to mass-production)
- Numerous patents and published technical papers
